REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-14 are pending in this application. Claim 1 is amended by the present response.

The changes to the claims are believed to find support in the disclosure as originally filed and thus are not believed to raise a question of new matter.

In the outstanding Office Action, Claims 1-8 and 12-14 are rejected under 35 U.S.C. § 102(e) as anticipated by Admitted Prior Art. Claims 9-11 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Initially, Applicants gratefully acknowledge the early indication of the allowable subject matter in Claims 9-11. However, since Applicants consider that amended Claim 1 patentably defines over the cited art, Claims 9-11 have presently been maintained in dependent form.

Before turning to the outstanding prior art rejections, it is believed that a brief review of the present invention would be helpful.

In this regard independent Claim 1 describes a plurality of memory cell arrays having memory cells arranged in a matrix, as shown in a non-limiting example in Figure 9 (Array 0-7). Further, Claim 1 describes that the plurality of memory cell arrays are independently located and each memory cell array is associated with a cell array group which includes two or more different memory cell arrays. For example in Figure 9, Array 0 and Array 4 could form one group as they are different arrays. Finally, Claim 1 describes that a Pass/Fail signal is output from each cell group. Thus, in Figure 9, the group including Array 0 and Array 4 outputs one Pass/Fail signal. For example, this is necessary because the 2-Gbit package product of Figure 9 is designed for two 1-Gbit chips and as such can only process four

Pass/Fail signals. Thus, in Figure 9 the pass signal of Array 0 and the pass signal of Array 4 are "or"ed to produce a single pass signal.

Turning now to the rejection of Claims 1-8 and 12-14 under 35 U.S.C. §102(e), Applicants traverse the rejection.

Claim 1 describes a semiconductor memory comprising "a plurality of memory cell arrays having a plurality of memory cells or memory cell units each of which include a plurality of memory cells, arranged in a matrix, wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more different memory cell arrays, and a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group."

The outstanding Office Action states that Admitted Prior Art describes, "a plurality of cell array groups each of which have two or more memory cell arrays, (in the instant case, the upper Array 0 and the lower Array 0 would be one cell array group..."[1]

However, the Admitted Prior Art does not describe or suggest a plurality of cell array groups each of which includes two or more different memory cell arrays, and a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group.

In other words, the "upper" Array 0 and "lower" Array 0 of Figure 2 are the same Array. Array 0 only produces one Pass/Fail signal. Thus, Array 0 is a group of only one memory cell array. In contrast, Claim 1 describes memory cell groups each of which includes two or more different memory cell arrays. In other words, the two or more independent and different memory cell arrays will produce two or more different Pass/Fail signals that must be grouped. Thus Claim 1 describes that a Pass/Fail signal is outputted in accordance with each cell array group (which includes a number a Pass/Fail signals)

[1] Office Action, dated 12/7/2005.

Accordingly, Applicants respectfully submit that Admitted Prior Art does not teach or suggest "a plurality of cell array groups each of which includes two or more different memory cell arrays, and a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group." as recited in Claim 1.

Therefore, it is respectfully submitted that independent Claim 1 and Claims 2-14 depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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